In the Claims

1. (Original) A computer system comprising:

a non volatile memory in which is stored a firmware error handling routine for handling errors; and

at least one processor wherein each of the at least one processors detects errors and executes the firmware error handling routine on detecting an error to handle the error and wherein the firmware error handling routine logs error information to a log.

2. (Original) The computer system of claim 1, wherein the error handling routine collects state information, saves the state information to the log, analyzes the error and attempts to correct the error.

3. (Original) The computer system of claim 1 wherein the firmware error handling routine analyzes the error and determines a severity of the error and handles a plurality of detected errors in order of the severity of the error.

4. (Original) The computer system of claim 2 further comprising:

a system memory in which is stored an operating error handling routine for handling errors; and

wherein the at least one processor executes the operating system error handling routine on failure to correct the error by the firmware error handling routine.

5. (Original) The computer system of claim 4, wherein the operating error handling routine attempts to correct the error by terminating processes affected by the error.

6. (Original) The computer system of claim 5, wherein the operating error handling routine reboots the system on failure to correct the error.

7. (Original) A computer system comprising:

a non volatile memory in which is stored a processor abstraction layer error handling routine and a system abstraction layer error handling routine; and

a processor coupled to the non volatile memory for executing the processor abstraction layer error handling routine and the system abstraction layer error handling routine on detecting an error.

8. (Original) The computer system of claim 7 further comprising:

platform hardware coupled to the processor, wherein the processor detects errors in the platform hardware as errors.

9. (Original) The computer system of claim 7, wherein error handling is cooperatively performed by the processor, the processor abstraction layer and the system abstraction layer.

10. (Original) The computer system of claim 9, wherein the system abstraction layer error handling routine analyzes the error and the state information, obtains additional state information by utilizing processor abstraction layer procedures, determines a severity of the error, creates a log containing the state information, and attempts to correct the error on processor abstraction layer being unable to correct the error.

11. (Original) A computer system comprising:

a plurality of systems comprising:

a non volatile memory in which is stored a first error handling routine and a second error handling routine; and

a processor coupled to the non volatile memory to execute the first error handling routine and the second error handling routine and to generate an error log on detecting an error.

12. (Original) A system for cooperative error handling comprising:

a memory in which is stored a first error handling routine for correcting errors and a second error handling routine for correcting errors; and

a detecting processor coupled to the non volatile memory to detect errors, to execute the first error handling routine on detecting an error, to execute the second error handling routine on failure of the first error handling routine to correct the error.

13. (Original) The system of claim 12, further comprising a system memory coupled to the detecting processor in which is a third error handling routine wherein the detecting processor executes the third error handling routine on failure of the first and second error handling routines to correct the error.

14. (Original) A system comprising:

a processor;

a system memory; and

a non-volatile memory in which is stored:

a first error handling routine executed on an error to access state information, store the state information to a log and to attempt to correct the.

15. (Original) The system of claim 14, wherein the non-volatile memory further comprises a second error handling routine branched to on completion of the first error handling routine, wherein the second error handing routine stores a status of the error and the state information to the log and attempts to correct the error.

16. (Original) The system of claim 15, wherein the system memory further comprises a third error handling routine executed by the processor on failure of the second error handling routine to correct the error, wherein the third error routine accesses the log and attempts to correct the error by terminating affected processes and wherein the first error handling routine is a processor abstraction layer error handling routine, the second error handling routine is a system abstraction

layer error handling routine and the third error handling routine is an operating system error handling routine.

17. (Original) The system of claim 16, wherein the third error handling routine causes the system to reboot on failure to correct the error.

18. (Canceled).

19. (Original) A method for handling errors in a system comprising:

detecting an error;

determining if the error is global or local;

on the error being global, signaling other processors of the error and allowing one processor to control error handling;

determining if the error is unrecoverable;

on the error being unrecoverable, halting the system;

correcting the error.

20. (Original) The method of claim 19, further comprising:

interrupting affected processes; and

resuming the affected processes after correcting the error.

21. (Original) The method of claim 19, further comprising:

saving state information; and

determining a severity of the error.

22-23. (Canceled)

24. (Original) A computer readable medium containing computer instructions for instructing a processor to perform a method for cooperatively handling errors comprising:

attempting to correct an error by a detecting processor;

on failure, executing firmware code to correct the error; and

on failure, executing operating system code to correct the error.

25. (Original) The computer readable medium containing computer instructions for instructing a processor to perform a method for cooperatively handling errors, further comprising:

on the operating system being a legacy operating system, sending compatible instructions to the operating system.

26. (New) A method for handling errors in a system having multiple processors, where:

any one of the processors detects an error;

a PAL error handler executes within the one processor that detected the error to

create an entry in an error log,

save state information,

attempt to diagnose and/or correct the error;

if the one PAL error handler fails to correct the error, a system abstraction layer (SAL) error handler attempts to correct the error in response to the error log entry and the saved state information.

27. (New) The method of claim 26 where the system-level error handler saves additional state information.

28. (New) The method of claim 26 where, if the system-level error handler fails to correct the error, an operating-system (OS) error handler attempts to correct the error in response to the error log entry and the saved state information.

29. (New) The method of claim 26 where the error log is common to multiple ones of the PALs.

30. (New) A data processing system, comprising:

an error log;

a plurality of processors to execute software processes and to detect errors;

a processor abstraction layer (PAL) error handler executable in one of the processors detecting an error to

create an entry in the error log,

save state information,

attempt to correct the error;

a system abstraction layer (SAL) error handler, responsive to failure of the one PAL error handler to correct the error, to attempt to correct the error in response to the error log entry and the saved state information.

31. (New) The system of claim 30 further comprising a non-volatile memory to store the PAL error handler.

32. (New) The system of claim 31 where the non-volatile memory also stores the SAL error handler.

33. (New) The system of claim 30 where the SAL error handler saves additional state information.

34. (New) The system of claim 30 further comprising an operating-system (OS) error handler responsive to failure of the system-level error handler to correct the error to attempt to correct the error in response to the error log entry and the saved state information.

35. (New) The system of claim 34 further comprising a system memory to store the OS error handler.

36. (New) The system of claim 30 where the error log is an expandable linked list.

37. (New) The system of claim 36 where the error log includes entries for past uncorrected errors.

38. (New) A data-processing system, comprising:

a plurality of processors to execute software processes and to detect an error;

an error handler executing in ones of the processors detecting the error, to diagnose and/or correct the error, to determine whether the error has a certain characteristic, and, if the error has the certain characteristic, to designate a particular one of the processors to execute the error handler for the entire system.

39. (New) The system of claim 38 further comprising an error log accessible by all of the error handlers.

40. (New) The system of claim 38 where the error handlers have at least two layers.

41. (New) The system of claim 40 where one of the layers is a processor abstraction layer (PAL).

42. (New) The system of claim 40 where one of the layers is a system abstraction layer (SAL).

43. (New) The system of claim 40 further comprising an operating-system (OS) error handler.

44. (New) The system of claim 38 where the certain characteristic is that the error is global and severe.

45. (New) The system of claim 38 where the certain characteristic is that a predetermined number of errors have occurred within a fixed period of time.